

CLAIMS

What is claimed is:

1 1. An intermediate microelectronic package, comprising:  
2 a first encapsulated die assembly having an active surface and a back surface, said  
3 first encapsulated die assembly including at least one first microelectronic die having an  
4 active surface and at least one side and a first packaging material adjacent said at least  
5 one first microelectronic die side; and  
6 a second encapsulated die assembly having an active surface and a back surface,  
7 wherein said second encapsulated die assembly back surface is attached to said first  
8 encapsulated die assembly back surface, said second encapsulated die assembly including  
9 at least one second microelectronic die having an active surface and at least one side and  
10 a second packaging material adjacent said at least one second microelectronic die side.

1 2. The intermediate microelectronic package of claim 1, wherein said first  
2 encapsulated die assembly active surface comprises said at least one first microelectronic  
3 die active surface and at least one surface of said first packaging material which is  
4 substantially planar to said first microelectronic die active surface.

1 3. The intermediate microelectronic package of claim 1, wherein said second  
2 encapsulated die assembly active surface comprises said at least one second  
3 microelectronic die active surface and at least one surface of said second packaging  
4 material which is substantially planar to said first microelectronic die active surface.

1 4. The intermediate microelectronic package of claim 1, further including at  
2 least one layer of dielectric material disposed over said first encapsulated die assembly  
3 active surface and at least one conductive trace extending through and residing on said at  
4 least one dielectric material layer.

1 5. The intermediate microelectronic package of claim 1, further including at  
2 least one layer of dielectric material disposed over said second encapsulated die assembly  
3 active surface and at least one conductive trace extending through and residing on said at  
4 least one dielectric material layer.

1 6. The intermediate microelectronic package of claim 1, further including an  
2 adhesive material disposed between said first encapsulated die assembly back surface and  
3 second encapsulated die assembly back surface.

1 7. The intermediate microelectronic package of claim 6, wherein said  
2 adhesive material is disposed in a desired patterned between said first encapsulated die  
3 assembly back surface and second encapsulated die assembly back surface.

1 8. The intermediate microelectronic package of claim 1, wherein said first  
2 and said second packaging material comprises an encapsulation material.

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1 9. The intermediate microelectronic package of claim 1, wherein said first  
2 and said second packaging material comprises a microelectronic package core and an  
3 encapsulation material.

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1 10. A method of fabricating microelectronic dice, comprising:  
2 providing a first encapsulated die assembly having an active surface and a back  
3 surface, said first encapsulated die assembly including at least one first microelectronic  
4 die having an active surface and at least one side and a first packaging material adjacent  
5 said at least one first microelectronic die side; and  
6 providing a second encapsulated die assembly having an active surface and a back  
7 surface, said second encapsulated die assembly including at least one second  
8 microelectronic die having an active surface and at least one side and a second packaging  
9 material adjacent said at least one second microelectronic die side; and  
10 attaching said first encapsulated die assembly back surface to said second  
11 encapsulated assembly back surface.

1 ~~2~~ 11. The method of claim ~~10~~, further including forming at least one layer of  
2 dielectric material over said first encapsulated die assembly active surface.

1 ~~3~~ 12. The method of claim ~~11~~, further including forming at least one conductive  
2 trace extending through and residing on said at least one dielectric material layer.

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4  
13. The method of claim 10, further including forming at least one layer of dielectric material over said second encapsulated die assembly active surface.

5 4  
14. The method of claim 13, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

6 1  
15. The method of claim 10, further including simultaneously forming at least one layer of dielectric material over said first encapsulated die assembly active surface and at least one layer of dielectric material over said second encapsulated die assembly active surface.

7 6  
16. The method of claim 15, further including simultaneously forming at least one conductive trace extending through and residing on said at least one dielectric material layer on said first encapsulated die assembly and at least one conductive trace extending through and residing on said at least one dielectric material layer on said second encapsulated die assembly.

8 1  
17. The method of claim 10, wherein said attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface comprises disposing an adhesive on said first encapsulated die assembly back surface and contacting said second encapsulated assembly back surface with said adhesive.

9 8  
1 ~~18~~ The method of claim ~~17~~, wherein said disposing an adhesive on said first  
2 encapsulated die assembly back surface comprises patterning said adhesive on said first  
3 encapsulated die assembly back surface.

10 9  
1 ~~19~~ The method of claim ~~18~~, wherein said patterning said adhesive comprises  
2 placing at least one adhesive line between a first microelectronic die and an adjacent  
3 microelectronic die on said first encapsulated die assembly back surface.

11 10  
1 ~~20~~ The method of claim ~~19~~, further including dicing said first encapsulated  
2 die assembly and said second encapsulated die assembly such that said dicing removes  
3 said at least one adhesive line.

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1 21. The method of claim 10, wherein said providing a first encapsulated die  
2 assembly comprises:  
3 providing at least one first microelectronic die having an active surface  
4 and at least one side;  
5 abutting a protective film against said at least one first microelectronic die  
6 active surface;  
7 encapsulating said at least one microelectronic die with an encapsulation  
8 material adjacent said at least one first microelectronic die side, wherein said  
9 encapsulation material provides at least one surface of said encapsulation material  
10 substantially planar to said first microelectronic die active surface; and

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included

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removing said protective film.

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The method of claim 10, wherein said providing a second encapsulated die

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assembly comprises:

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providing at least one second microelectronic die having an active surface

4

and at least one side;

5

abutting a protective film against said at least one second microelectronic

6

die active surface;

7

encapsulating said at least one microelectronic die with an encapsulation

8

material adjacent said at least one second microelectronic die side, wherein said

9

encapsulation material provides at least one surface of said encapsulation material

10

substantially planar to said second microelectronic die active surface; and

11

removing said protective film.

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23. A method of fabricating a microelectronic package, comprising:

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forming a first encapsulated die assembly comprising:

3

providing at least one first microelectronic die having an active

4

surface and at least one side;

5

abutting a protective film against said at least one first

6

microelectronic die active surface; and

7

encapsulating said at least one microelectronic die with an

8

packaging material adjacent said at least one first microelectronic die side

9 to form a first encapsulated die active surface and a first encapsulated die  
10 back surface;  
11 forming a second encapsulated die assembly comprising:  
12 providing at least one second microelectronic die having an active  
13 surface and at least one side;  
14 abutting a protective film against said at least one second  
15 microelectronic die active surface; and  
16 encapsulating said at least one microelectronic die with an  
17 packaging material adjacent said at least one second microelectronic die  
18 side to form a second encapsulated die active surface and a second  
19 encapsulated die back surface; and  
20 attaching said first encapsulated die assembly back surface to said second  
21 encapsulated assembly back surface.

1 <sup>15</sup>  
~~24.~~ The method of claim <sup>14</sup>~~23~~, further including forming at least one layer of  
2 dielectric material over said first encapsulated die assembly active surface.

1 <sup>16</sup>  
~~25.~~ The method of claim <sup>14</sup>~~23~~, further including forming at least one conductive  
2 trace extending through and residing on said at least one dielectric material layer.

1 <sup>17</sup>  
~~26.~~ The method of claim <sup>14</sup>~~23~~, further including forming at least one layer of  
2 dielectric material over said second encapsulated die assembly active surface.

1 <sup>18</sup>  
~~27.~~ The method of claim <sup>14</sup>~~23~~, further including forming at least one conductive  
2 trace extending through and residing on said at least one dielectric material layer.

1 <sup>19</sup>  
~~28.~~ The method of claim <sup>14</sup>~~23~~, further including simultaneously forming at least  
2 one layer of dielectric material over said first encapsulated die assembly active surface  
3 and at least one layer of dielectric material over said second encapsulated die assembly  
4 active surface.

1 <sup>20</sup>  
~~29.~~ The method of claim <sup>19</sup>~~28~~, further including simultaneously forming at least  
2 one conductive trace extending through and residing on said at least one dielectric  
3 material layer on said first encapsulated die assembly and at least one conductive trace  
4 extending through and residing on said at least one dielectric material layer on said  
5 second encapsulated die assembly.

1 <sup>21</sup>  
~~30.~~ The method of claim <sup>14</sup>~~23~~, wherein said attaching said first encapsulated die  
2 assembly back surface to said second encapsulated assembly back surface comprises  
3 disposing an adhesive on said first encapsulated die assembly back surface and contacting  
4 said second encapsulated assembly back surface with said adhesive.



1 <sup>22</sup>  
~~31.~~ The method of claim <sup>21</sup>~~30~~, wherein said disposing an adhesive on said first  
2 encapsulated die assembly back surface comprises patterning said adhesive on said first  
3 encapsulated die assembly back surface.

1 <sup>23</sup>  
~~32.~~ The method of claim <sup>22</sup>~~31~~, wherein said patterning said adhesive comprises  
2 placing at least one adhesive line between a first microelectronic die and an adjacent  
3 microelectronic die on said first encapsulated die assembly back surface.

1 <sup>24</sup>  
~~33.~~ The method of claim <sup>23</sup>~~32~~, further including dicing said first encapsulated  
2 die assembly and said second encapsulated die assembly such that said dicing removes  
3 said at least one adhesive line.

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